Radiation Effect Characterization and Test Methods of Single-Chip and Multi-Chip Stacked 16Mbit DRAMs

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Abstract

This paper presents radiation effects characterization performed by the NASA Goddard Space Flight Center (GSFC) on spaceflight candidate 16Mbit DRAMs. This includes heavy ion, proton, and Co60 irradiations on single-chip devices as well as proton irradiation of a stacked DRAM module. Lastly, a discussion of test methodology is undertaken.

I. Introduction

Commercial dynamic random access memory (DRAM) devices are increasingly in demand as memory storage devices on spacecraft due to their high device density and superior performance characteristics. Today, denser cell structures are desired by spaceflight designers to fulfill increasingly higher mission data storage requirements, making the DRAM an inviting choice. In addition, recent technology has permitted the "stacking" of these devices into a single module providing even denser packaging of DRAMs into a single "device". However, due to the reduction in device geometry and the use of commercial components with potentially troublesome radiation-induced charcteristics, a comprehensive test program was undertaken to determine the radiation sensitivity of both single DRAM devices as well as a stacked configuration.

Single event effect (SEE) and total ionizing dose (TID) testing was performed on several candidate DRAMs. One candidate DRAM was selected for use in a stacked configuration, producing a dense memory module. Proton testing was performed on this module to resolve questions about potential proton penetration throughout the package, as well as secondary effects.

II. Background

Previously flown static random access memory (SRAM) devices have been analyzed for in-flight performance, including the 256 kbit and 1 Mbit Hitachi SRAMs utilized on CRUX, TOMS/Meteor-3, TOPEX, and SAMPEX [Ref 1,2]. These devices were tested for radiation-induced failure modes in pre-flight tests and results were compared with in-flight data. Several 16 Mbit DRAM (4Mx4) devices tested in this program are currently being designed into solid state recorders (SSRs) on the Hubble Space Telescope Tape Recorder Replacement, Landsat-7, and TRACE Missions, as well as on several non-NASA spaceflight projects.

III. Radiation Test Program

A. Device Characteristics and Test Chronology

Table 1 presents the devices tested and salient characteristics, as measured during testing.

Table 1 Salient 4Mx4 Device Characteristics

Manufacturer	**Part Number**	**Technology**	**V_{CC} in V(typ)**	**LDC**	**Power in W (Stdby)**	**Power in W (Active)**	**Access Time**
Fujitsu	8116400-60PJ	CMOS	5	9337	8mW	85mW	60ns
Hitachi	HM5116400AJ7	CMOS	5	9447	8mW	77mW	60ns
Hitachi	HM5117400RR7	CMOS	5	9236	8mW	75mW	70ns
IBM	43G9240 (Luna ES DD2 or Rev B)	CMOS	3.3	9314	< 3mW	26.5mW	70ns
IBM	0116400PT1C-70 (Luna ES DD3 or Rev C)	CMOS	3.3	63G6545	< 3mW	23mW	70ns
IBM	0116400J1B-70 and TP0116400AJ3B-70 (Luna ES	CMOS	5	9314	< 5mW	40mW	70ns

	DD2 or Rev B)						
IBM	0116400J1C-70 (Luna ES DD3 or Rev C)	CMOS	5	43G6569	< 5mW	35mW	70ns
Micron	4MT4CM4B1W	CMOS	5	9404	8mW	85mW	70ns
Motorola	MCM516400J60	CMOS	5	9331	N/A	N/A	60ns
NEC	D4216400G3-70	CMOS	3.3	9449	8mW	60mW	70ns
NEC	4216400-70	CMOS	5	9409	8mW	75mW	70ns
Samsung	KM44C4000AJ-7	CMOS	5	4084	8mW	70mW	70ns
Toshiba	TC5117400FT-70	CMOS	5	N/A	8mW	90mW	70ns
Toshiba	TB5117400J-6	CMOS	5	YB4927	8mW	85mW	60ns

In mid-1994, NASA GSFC began investigating 16Mbit DRAMs. Several of the devices were tested in heavy ion and proton test chambers. Heavy ion SEE testing was performed on Fujistu, Micron, Samsung, and two Toshiba DRAMs at Brookhaven National Laboratory's Twin-Tandem Van de Graaff accelerator. Proton SEE testing was perfomed on the Fujistu, Hitachi, Toshiba and Motorola devices at the Univeristy of California at Davis' Crocker Nuclear Laboratory proton cyclotron. Results showed that some DRAMs were potentially usable in the single event effect environment.

In 1995, several NASA spacecraft had baselined SSR designs that included specific 16Mbit DRAMs. Thus, the IBM rev B, Hitachi, and NEC devices were tested for SEE susceptibility to protons and, in some cases, TID. Newer versions of the devices, or "die shrinks", were also tested to ensure survivability. Heavy ion tests were then performed on the IBM rev C DRAM.

Lastly, to ease the concern about secondary particle and propagated effects inside a stacked module from high energy proton strikes, a 160 Mbit DRAM stack, courtesy of Irvine Sensors [Ref 3], consisting of ten IBM rev C DRAMs was tested at the Indiana University Cyclotron Facility.

Portions of this data have been presented previously [Ref 4]; this data has been reanalyzed here,

to adjust for changes in the test setup allowing capture of more data. These changes are explained in Part C, SEE Test Methods, below.

B. Types of SEEs

Observed SEE results include the standard single bit upset errors (standard SEU), column or row address errors (where a single ion strike induces a partial or full address column or row to be in error in a single device), single event functional interrupt (SEFI), "stuck bits" (bits unable to be reprogrammed after irradiation), and single event latchup (SEL). Row and column errors are often referred to as block errors for simplicity. Multiple bit upsets (MBU), when a single ion strike induces multiple bits to upset inside a single data structure, were neither observed nor expected in these devices due to the physical device layout. In this case, the adjacent cells within the device correspond to different logical and physical nibbles, bytes, words, etc.

C. SEE Test Methods

Several test modes, both dynamic and static, were utilized during SEE irradiations. Accesses by individual bytes and by pages (groups of bytes) were performed. These modes are listed in Table 2 below.

Table 2 SEE Test Results for 16 Mbit DRAMs

DRAM access type	**Access mode**	**Description**
Dynamic	Write byte	During irradiation, device is written on a byte-by-byte basis. Memory cell contents verified post-irradiation
Dynamic	Write page	During irradiation, device is written on a page-by-page basis. Memory cell contents verified post-irradiation
Dynamic	Read-Modify-Write Byte	Prior to irradiation, device is loaded with a test pattern. During irradiation, device is read continuosly, errors noted and corrected by a byte write.
Dynamic	Read-Modify-Write Page	Prior to irradiation, device is loaded with a test pattern. During irradiation, device is read continuosly, errors noted and corrected by a page write.
Static	RAS or CBR refresh only*	Prior to irradiation, device is loaded with a test pattern. During irradiation, device is refreshed within device specifications. Memory cell contents verified post-irradiation.

* Note: RAS is row-address refresh; CBR is CAS (column-address refresh) before RAS

Test patterns utilized include all ones, all zeroes, and checkerboard. Power supply voltages for SEU testing were nominally V_{CC} and V_{CC}-10%, while for SEL testing V_{CC} and V_{CC}+10% were used.

Tests performed in 1994 did not capture address information, hence, block errors were not characterized or noted. All tests since have captured full address and data information of error occurance to allow for more complete analysis. Please note that for this reason, data presented here may differ from that presented in [Ref 4].

D. TID Test Methods

TID testing was performed utilizing a Co-60 source at NASA GSFC[Ref 4,5]. All testing was performed at low dose rates (between 0.01-0.3 rads (Si)/second) using Mil-883 Group E test methods. Testing was performed for full parametrics such as I_{cc}, V_{OL}, V_{OH}, I_{IH}, I_{IL}, etc., while functional tests utilized simple and complex test patterns such as all ones, all zeroes, checkerboard, et al. Failure levels were noted both when the first device exceeded parametric specifications or showed functional failure, as well as when all devices failed either parametric or functional tests.

IV. Test Results

A. SEE Results

SEE heavy ion and proton test results are summarized in Table 3. Heavy ion results are presented according to the linear energy transfer or LET threshold (LET_{th}), which represents the LET of the first event observed at a fluence of $1x10^7$ particles/cm^2. All units for LET are described in MeV*cm^2/mg. Proton results are presented according to proton energy in MeV.

Table 3 SEE Heavy Ion and Proton Test Results Summary

Test Type	**Test Date**	**Manufacturer**	**Part Number**	**SEU LET_{th} / sigma @ $(LET)^+$**	**SEL LET_{th} / sigma @ (LET)**	**Other**
heavy ion	5/4/94*	Fujitsu	8116400-60PJ	< 1.41 / 3 cm^2/device (80)	> 80 / NA	-
proton	5/24-25/94*	Fujitsu	8116400-60PJ	-	-	Proton sigma=1.2E-7 cm^2/device @ 63 MeV

proton	3/24-25/95	Hitachi	HM5116400AJ7	-	-	Cell sigma=2E-7 cm^2/device @ 63 MeV
proton	5/24-25/94*	Hitachi	HM5117400RR7	-	-	Proton sigma=3.6E-7 cm^2/device @ 63 MeV
proton	3/24-25/95	IBM	43G9240 (rev B)	-	-	Cell sigma=6E-9 cm^2/device @ 63 MeV, block errors
proton	5/4-5/95	IBM	0116400PT1C-70 (rev C)	-	-	Cell sigma=< 2E-9 cm^2/device @ 63 MeV, block errors
proton	3/24-25/95	IBM	0116400J1B-70 (revB)	-	-	Cell sigma=6E-9 cm^2/device @ 63 MeV, 1 block error
proton	5/4-5/95	IBM	0116400J1C-70 (rev C)	-	-	Cell sigma=< 2E-9 cm^2/device @ 63 MeV
heavy ion	6/5/95	IBM	0116400J1C-70 (rev C)	~3 / 7E-2 cm^2/device (50)	> 50 / NA	block errors @ LET=5
heavy ion	8/16-18/95	IBM	0116400J1C-70 (rev C)	-	-	Special test - see text
proton	9/5-8/95	Irvine Sensor 160 Mbit stacks	0116400J1C-70 (rev C)	-	-	No SEUs seen, though expected based on single chip tests
heavy ion	5/4/94*	Micron	4MT4CM4B1DW	< 1.41 / > 2E-1 cm^2/device (12)	between 12.2 and 26.6 / 2E-4 cm^2/device (50)	-
proton	5/24-25/94*	Motorola	MCM516400J60	-	-	Proton sigma=1.2E-6 cm^2/device @ 63 MeV
prot	5/24-	Motorola	MCM517	-	-	Proton sigma=1.2E-6

on	25/94*		400J60			cm^2/device @ 63 MeV
proton	5/4-5/95	NEC	D4216400G3	-	-	Cell sigma=2E-7 cm^2/device @ 63 MeV
proton	3/24-25/95	NEC	4216400-70	-	-	Cell sigma=5E-7 cm^2/device @ 63 MeV, 4 test runs
heavy ion	7/29-8/1/94*	Samsung	KM44C4000AJ-7	< 1.46 / 3 cm^2/device (110)	>110 / NA	SEFI at LET=59.6, stuck bits @ LET=59.6
proton	5/24-25/94*	Toshiba	TC5117400FT-70	-	-	Proton sigma=1.5E-6 cm^2/device @ 63 MeV
heavy ion	7/29-8/1/94*	Toshiba	TC5117400J-6	< 1.46 / 3 cm^2/device (100)	> 100 / NA	-

* For tests before '95, block errors were not captured.
+ Sigma is the device's sensitive cross section.

B. TID Results

TID testing was performed on the IBM rev B and rev C DRAMs [Ref 5,6]. Both device types passed the 20 kRad(Si) cumulative irradiation mark without signs or parametric or functional degradation. The rev C devices exhibited parametric failures on I_{IH} and I_{OZH} measurements at the 30 kRad(Si) mark, and functional failures at the 75 kRad(Si) level. The rev B devices did not exhibit parametric degradation until the 50 kRad(Si) level (V_{IH} and V_{IL}). Functional failures on the rev B were not observed until after the devices were annealed at room temperature for 168 hours after 100 kRad(Si) dose irradiation.

V. Discussion of SEE Test Results

A. Effect of mode on device results

Test results showed little or no dependence on the test mode (dynamic or static) or access method (byte or page) utilized. Intuitively, this makes sense. When the device is not being written to or read from, refreshing of memory cells is typically required. Thus, even in a static (data storage) mode, cell access through memory refresh cycles is being performed.

B. SEL

SEL was observed on only one device during heavy ion testing: the Micron DRAM. Current exceeded 80 mA during SEL occurrence beginning at an LET between 12.2 and 26.6.

C. Memory cell errors

All devices that were tested exhibited high sensitivity to standard single bit errors in memory cells. As one would expect, these commercial DRAMs are very soft to SEUs. With the exception of the IBM rev C device, the other four device types tested for heavy ions had $LET_{th} < 1.46$, with maximum experimentally determined device cross-sections approaching the actual device physical area. The IBM rev C DRAM had a maximum measured cross-section approximately 1.5 orders of magnitude smaller than the other tested DRAMs with an LET_{th} of 3. Figure 1 illustrates a sample of the heavy ion test data for the IBM rev C.

Proton SEU results were similiar; devices were very sensitive to proton-induced SEUs. Again, the IBM devices (rev B and C) were 2 orders of magnitude less sensitive to upset than the other devices.

No pattern dependence or MBUs were observed on any test sample during any test.

D. SEFI

SEFI was observed on the Samsung device. When SEFI occurred, the device appeared to enter a test or standby (low power) mode of operation that required either a reinitialization or a power cycling to recover. SEFI was first observed when tested with Iodine at normal incidence.

E. Stuck bits

Stuck bits were observed on the same Samsung device with Iodine at normal incidence, at an energy of 305 MeV and an LET of 59.6. Memory cells that exhibited this phenomenon could not be reprogrammed to the opposite value following the event.

E. Block errors

Block errors appear as a physical column or row inside a DRAM exhibiting a large number of errors in that column or row address. The test setup was modified in early 1995 to detect this event. Hence, less than half the device types in this experiment were tested for block errors.

With that limited scope, both the IBM rev B and C devices exhibited block errors. Heavy ion results for the rev C 5V version showed a LET_{th} of 5. Proton results are discussed in the next section.

F. Results of 5V versus 3.3V Devices

The IBM Luna-ES rev B and rev C are internally mask-configurable to operate as a 3.3V or 5V device. All the memory cells in both versions operate at 3.3V. An internal ring of voltage converters interface between the outside world and the memory cells is enabled during 5V operation. Design of the voltage converters is proprietary.

During proton irradiation, cell error rates were comparable for both voltage variations. This is as expected, since all internal memory cells operate at 3.3V. However, as seen in Figure 2, the 3.3V versions were more sensitive to power supply variation (i.e., the device became more sensitive to SEE as voltage was reduced) than the 5V version. The internal regulator that is enabled on the 5V devices keeps the internal V_{CC} to 3.3V for the memory cells even when the external power supply voltage is reduced to 4.5V. The 3.3V device results appear fairly linear with this power supply variance, as one might expect.

Additionally, several block errors were observed on the 3.3V version, but not on the 5V. Preliminary analysis indicates a potential internal capacitive coupling with the device's ground plane depending on whether the 5V regulators were enabled, i.e., an energetic particle strike coupling noise to a ground plane internal to the device [Ref 7].

G. Variance of Refresh Rate

Several test runs were performed during proton irradiation of the IBM rev B and C devices with varying refresh cycle times. Although insufficient data was gathered for full statistical analysis, the results from 8 to 256 msec cycle times exhibited little difference in memory cell or other SEUs.

H. Stacked DRAM Results

No SEEs were observed - though they were expected based on the previous rev C single-chip test - during proton testing of this device at energies up to 197 MeV (more than sufficient in terms of penetration range for even these stacked die). The preliminary theory for this result (currently being further explored) is a variance in the capacitive levels between the single-chip and multi-chip module (MCM) devices. Also, the single-chip test sets might have more (albeit within device specification) coupled noise than that internal to the MCM. Inside the MCM, die are stacked and connected in a manner different from when they are in single IC packages. In discussions with the stack manufacturer, capacitance (hence noise immunity) will be different as well [Ref 8]. This might well be important in future investigations.

I. Preliminary Data on IBM LUNA ES2 4Mx4 DRAM

Recent proton and limited heavy ion test data has been gathered on the IBM Luna ES2 (DD4) DRAM device. We shall provide, for completeness, a brief synopsis herein.

Two versions (5 and 3.3V) were irradiated with protons, while, due to packaging constraints, only the 5V device was tested with heavy ions. Part numbers and data codes were 0116400BJ1D-70, 9352 (3.3V) and 0116400J1D-70, 9314 (5V). These devices had unkown redesigns from the Luna ES rev C devices.

Preliminary data shows that both these devices are more susceptible to cell errors than the ES devices. The experimental device cross-section for protons of the 5V device was ~$2x10^{-8}$2, an order of magnitude greater than for the ES versions. The 3.3V device exhibited similiar results with a 20-50% smaller device cross-section than the 5V DRAM. Column address (block) errors

were exhibited by the 5V device, but not the 3.3V. Laser SEU testing is planned to determine this result's cause. As with the ES 3.3V devices, the 3.3V ES2's exhibited a linear variance with power supply voltage versus device error cross-section.

Preliminary heavy ion testing on the 5V ES2 concurred with the proton irradiation; memory cell error cross-section was higher than for the ES 5V device. LET_{th} was ~ 3. As illustrated in Figure 3, block error sensitivity was also higher for the ES2 device than for the similiar ES device. The observed LET_{th} was 4 with a block error cross-section of ~$2x10^{-4}$ cm^2 per device at an LET of 12. No signs of SEFI or SEL were noted. Further testing at LETs higher than 12 is planned for the near future.

VI. Test Methodology Discussion

A. Impact of Method on Test Results

An anomolous condition, best described as a "stuck block error" (hereafter called a block SEFI), had been observed by other test organizations in the IBM Luna-ES rev C device during heavy ion testing [Ref 9]. When this anomaly occurs, an entire row of 1024 addresses has data values stuck at FFH. A simple writing of new data to the stuck row would not clear the problem, but a series of device refresh cycles would.

When this anomaly was observed, the test method was as follows; a page write operation of the entire device was performed (approximately 8 seconds), then each memory cell is read (with a modify-write if the cell value was incorrect) and compared to known good data. No refresh of memory cells was performed during the write cycle. When these block SEFIs occurred, this test set then issued 2 or more RAS only or CAS before RAS (CBR) refreshes to clear the problem.

As a followup experiment, GSFC and APL teamed to evaluate this anomaly. Several test modes using Page mode access were utilized:

Mode 1:

Write a Page
Refresh entire device (RAS or CBR)
Read page and check for SEFI blocks
If no SEFI blocks (1024 row address errors), repeat
Else Refresh Device (RAS or CBR) until SEFI block disppears

Mode 2:

Write a Page
Wait N (milli) seconds (N=8 seconds simulates test method where anomaly observed)
Read page and check for SEFI blocks
If no SEFI blocks (1024 row address errors), repeat
Else Refresh Device (RAS or CBR) until SEFI block disppears

Mode 3:

Write a Page
Wait N (milli) seconds
Refresh entire device (RAS or CBR)
Read page and check for SEFI blocks
If no SEFI blocks (1024 row address errors), repeat
Else Refresh Device (RAS or CBR) until SEFI block disppears

Testing was performed with a Br-79 ion, energy of 276 MeV with a LET at normal incidence of 37.4 MeV*cm^2/mg. Maximum fluence for test runs were 1x10^7 particles/cm^2. This ion was selected due to the occurrence of the stuck blocks at this LET and lower during the reported testing by another organization. In summary, multiple results were observed.

As long as periodic single RAS or CBR refreshes were performed with a refresh time value within the device specification of 64 msec up to a maximum tested time between refreshes of 1 refresh per 8 seconds, no block SEFIs were observed (Modes 1 and 3).

If write-only refreshes (i.e., the DRAM supposedly is refreshed in the same manner when a write occurs as when a RAS or CBR refresh occurs) are utilized as per Mode 2, block SEFIs then occur. Writes, apparently, do not refresh the device the same way that RAS or CBR refresh does.

When block SEFI occurs, a single RAS or CBR refresh to the device cleared the condition in 14 out of 15 test run occurences. 2 RAS's were utilized to clear the lone anomolous run. The reported data had stated that the DRAM required 2 to 8 refresh cycles to clear the anomaly.

The error cross section for block SEFI is approximately 1x10^{-6} cm^2. It should be noted that, several block SEFIs first appeared as less than 1024 stuck addresses, i.e., 722 stuck addresses would occur for several write-read cycles until 1024 bad addresses were noted.

The bottom line is this: the device must be active (write mode) with no device refreshes (RAS or CBR) occuring periodically for block SEFI to occur. This is out of specification for the device. In a typical spacecraft SSR usage, a write only occurs about once every few hours with device refresh occurring within device specification (along with potential Error Detection and Correction (EDAC) memory scrubbing). Thus, as long as the RAS or CBR refreshes are utilized to operate the device within specification, no block SEFI will occur.

VII. IMPLICATIONS FOR DESIGN OPTIONS

As has been previously noted [Ref 10], single bit errors and multiple bit errors in data structures may be handled by a system designer utilizing standard EDAC techniques such as Hamming codes or Reed-Solomon codes. The question then becomes, to what extent do these other anomalous conditions such as stuck bits or SEFI affect the designer.

Stuck bits, as long as they don’t occur with great frequency, may be treated in a similiar manner to single bit errors. The EDAC code would detect them and correct them. The Samsung device,

which exhibited this anomaly, has a low probabilty of ocurrence even in a worst case environment, so this is a non-issue for most spaceflight programs.

SEFI events provide a more complicated problem. Detecting and correcting such an event is a challenge for even the most experienced designer. Unlike SEL, device current consumption remains within normal operating conditions (or even lower if a standby mode is entered). The only apparent symptom is incorrect data when accessing the device. Take, for example, the Samsung device and its SEFI in a normal SSR application. Usually, the SSR organizes its data structures into 32-bit wide or larger structures. When a single 4Mx4 DRAM experiences SEFI, only 4 bits in that data structure are in error from the event assuming the the 32-bit word is spread across 8 devices. Standard Hamming EDAC would detect this error, but a more powerful EDAC code such as Reed-Solomon would be required to correct it. If a complex software or ground-based method is employed that keeps track of where (device/physical addresses) errors are occurring, it is possible to separate the SEFI from a simple four-bit error and to take appropriate action.

Block errors may be treated in a similiar manner as SEFI. Reed-Solomon class of EDAC codes will correct the data, but a more complex scheme is required to correct the cause of the errors.

VIII. RECOMMENDATIONS

With the exception of the Micron device which exhibited destructive SEL, no other device exhibited characteristics that may rule out their utilization in space. However, only the IBM rev B and C devices were fully characterized for SEE and TID. Thus, the recommendation for SSR applications is to utilize the IBM rev C devices in the 5V variation for missions with a proton-dominated orbits. This device did not exhibit any anomaly other than single bit errors due to protons, as wll as being relatively TID tolerant. For other orbits and applications, further system design/complexity tradeoffs should be addressed.

IX. CONCLUSION

Radiation sensitivity of commercial DRAMs ranged from extremely sensitive to moderate. With proper test methodology, mitigative techniques such as EDAC, and packaging methods, successful use of some of these devices is viable for spacecraft missions.

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